REMARKS

The title of the invention is objected to. Applicants have amended the title of the invention in accordance with the Examiner's request.

Claims 1-46 are rejected under 35 USC §112, first paragraph, as failing to comply the enablement requirement.

The Examiner states that it is unclear how the apparatus of FIG. 7 is interconnected and associated with the apparatus of FIGs. 1-6. The Pin Driver architecture that is described for FIG. 7 is built around the linear output stage described in FIGs. 4-6. By itself, the linear output stage of FIGs. 4-6 offers waveform fidelity and timing accuracy impossible to achieve with switched current designs. Combined with the drive circuitry presented in FIG. 7, signal propagation delay through the driver is independent of output amplitude, rise and fall times are matched without trimming, and rise and fall transitions are fully symmetrical. Moreover, the rise and fall signal propagation delays are matched without trimming and the rise and fall times are independent of output amplitude.

Note that the output of the Pin Driver described in FIG. 7 is similar to the linear output stage described in FIG. 6. Also, the input to the Pin Driver described in FIG. 7 is an input pulse train. The Pin Driver described in FIG. 7 is an alternate embodiment of the system described in FIGs. 1-6.

Secondly, the Examiner states that the specification does not have sufficient information about "a controlled cascode translinear multiplier cell configuration" and "low distortion means for controlling the amplitude." The CCGS 410 is an example of a controlled cascode

translinear multiplier cell configuration, as shown in FIG. 9. In other words, the arrangement shown in FIG. 9 is a cascode translinear multiplier cell configuration. The low distortion means is associated with the fact that elements Q1, Q2, Q3, Q4, Rg, R1, R2, I1 and I2 form a standard cascoded differential amplifier with fixed transresistance. As described in the specification, the transresistance of the cell is $R_g/1\text{-}I_{GAIN}/(I1+I2)$, which provides the CCGS 410 a very linear control gain control of the amplitude while maintaining high signal integrity.

Claims 1-46 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 1 and 19, the Examiner states that the terms "high speed slave chain" and "DC control loop" are unclear as to determining whether they are interconnected with a controller or controlling means. The Examiner further states that the terms "controller" or "controlling means" are unclear.

Note in FIG. 7 the inputs D and DB the driver circuit. The high speed slave (HSS) chain receives as input differential logic inputs D and DB, as described in FIGs. 1-6, from a controlling means. Moreover, the DC control loop (DCCL) provides DC regulation for the HSS chain. The term the controller or controlling means can be a processor associated with the main test system or console 12, as recited on page 7, line 4. Therefore, the controller or controlling means is shown in FIG. 1 and is not ambiguous. Applicant respectfully requests that the Examiner reconsider his position.

As for claims 9, 27, and 45, the Examiner states that the terms "a controlled cascode translinear multiplier cell configuration" and "low distortion means for controlling the amplitude" are unclear as to what they represent. FIG. 9 shows a controlled cascode translinear multiplier cell configuration. The low distortion means is associated with the fact that elements Q1, Q2, Q3, Q4, Rg, R1, R2, I1 and I2 form a standard cascoded differential amplifier with fixed transresistance. As described in the specification, the transresistance of the cell is $R_g/1\text{-}I_{GAIN}/(I1+I2)$, which provides a very linear control gain control of the amplitude while maintaining high signal integrity.

With respect to claims 11 and 29, the term "driver" has been amended to "driver circuit."

With respect to claims 13 and 31, the Examiner states that the terms "a differential input pair of transistors" are unclear as to what they represent. FIG. 10 shows the differential input pair of transistors as Q3 and Q4

With respect to claims 14 and 32, the Examiner states that the terms "pair of transistors that each receive a single ended voltage signal" are unclear as to what they represent. FIG. 10 shows the pair of transistors as Q1 and Q2, each receive a single ended voltage signal, D and DB.

With respect to claims 15 and 33, the Examiner states that the term "a resistance" is unclear. FIG. 10 shows the resistance as being RG.

With respect to claims 17 and 35, they have been canceled.

With respect to claim 34, the Examiner states that the terms "a pair of current sources" are unclear as to what they represent. FIG. 10 shows the pair or current sources as I1 and I2.

With respect to claim 37, claim 37 has been amended to address the Examiner's concern.

In view of the above amendments and for all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the objections and rejections made under 35 USC §112, first and second paragraphs. Accordingly, an early indication of allowability is earnestly solicited.

If the Examiner has any questions regarding matters pending in this application, please feel free to contact the undersigned below.

Respectfully submitted,

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